UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/273,560	03/22/1999	TAKUMI HASEGAWA	Q53743	7269

7590 05/13/2009

SUGHRUE, MION, ZINN, MACPEAK & SEAS
2100 PENNSYLVANIA AVE. N.W.
WASHINGTON,, DC 200373202

EXAMINER	
THANGAVELU, KANDASAMY	

ART UNIT	PAPER NUMBER
2123	

MAIL DATE	DELIVERY MODE
05/13/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Advisory Action Before the Filing of an Appeal Brief	Application No.	Applicant(s)	
	09/273,560	HASEGAWA, TAKUMI	
	Examiner	Art Unit	
	KANDASAMY THANGAVELU	2123	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 23 April 2009 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☒ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:

   a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.

   b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).

4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).

5. ☐ Applicant's reply has overcome the following rejection(s): _____.

6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).

7. ☒ For purposes of appeal, the proposed amendment(s): a) ☒ will not be entered, or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.
   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: 1-6.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).

9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).

10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See the attachment below.

12. ☐ Note the attached Information *Disclosure Statement*(s). (PTO/SB/08) Paper No(s). _____

13. ☐ Other: _____.

/Paul L Rodriguez/
Supervisory Patent Examiner, Art Unit 2123

Applicant's arguments with respect to claim rejections under 35 USC 112 First paragraph are not persuasive. Claim rejection under 35 USC 101 is maintained for claim 3, since none of the steps is indicated to be implemented on a computer. Applicant's arguments with respect to claim rejections under 35 USC 103 (a) are not persuasive.

As per the Applicants argument that "the Examiner asserts that the middle column of FIG. 3 ('Rise/fall') is incorrect; that the determination that no delay ('NONE') was caused by the input, as recited in claim 6, is incorrect; Applicants disagree; as discussed in the Specification, since the state of the output is low both at the first clock signal (when input 1 rises), and at the second clock signal (when input 2 falls), it is determined that no delay was caused by the input (Specification, page 7, line 22 to page 8, line 6, and FIG. 3); as such, the determination of 'NONE" in FIG. 3 is justified", the Examiner reaffirms his position in the Final rejection that the determination that no delay was caused by the input is incorrect.

As per the Applicants argument that "in the case where the input 1 rises and the input 2 falls, no change in a signal state of an output terminal of the logical circuit is determined (see FIG. 3, middle column- 'Rise/fall'); the delay analyzing module determines that no further delay analysis needs to be performed; this determination is automatic since it is based on the logical operation information of the logical circuit; therefore, Applicants submit that claim 5 complies with the requirements of 35 U.S.C. § 112", the Examiner reaffirms his position in the Final rejection that Claim 5 does not have support in the specification, as explained below.

The logical operation information does not have the capability to automatically determine based on the logical operation information of the circuit that there is no change in a signal state of an output terminal of the logical circuit. The applicant has not shown anywhere in the specification the existence of such capability. The applicant has not shown support in the specification for "when no change in the signal state is determined, the delay analysis module determines that no further delay analysis is needs to be performed". Specification Page 7, Line 22 to Page 8, Line 6 and Figs. 3-5 do not support the above features. In Fig. 3, the showing of "NONE" when input 1 rises and input 2 falls is incorrect. It is not understood as to how the applicant select "NONE". In the AND circuit, the delay is determined by the input rising later and the input falling earlier. Therefore, under Rise/Fall, the delay is determined first by input 1 that rises last and then by input 2 that falls earlier. This is what is done automatically.

As per the Applicants argument that "the features of claim 6 are supported by the Applicants' disclosure; claim 6 recites that … the delay time information of the AND gate is labeled as NONE indicating no change in the signal state at the output terminal of the AND gate, and the delay analyzing module, automatically determines that no further delay analysis needs to be performed; … claim 6 complies with the requirements of 35 U.S.C. § 112", the Examiner reaffirms his position in the Final rejection that Claim 6 does not have support in the specification, as explained in the paragraph above.

As per the Applicants argument regarding claim rejection under 35 USC 101, the Examiner takes the position that though the preamble of claim 3 indicated that the method is computer implemented, none of the steps is indicated to be implemented on a computer. Therefore, the Examiner maintains rejection of claim 3 under 35 USC 101.

As per the Applicants argument that "the logical operation does not teach or suggest all the features of the claimed logical operation information; the claimed logical operation information comprises delay time information which is specific to an input terminal logical state transition and a resulting logical state transition at an output terminal; Hasegawa ' 168 does not teach or suggest that the stored delay time is specific to a state transition of the pin; neither Hasegawa '511 nor Hasegawa '168 teach that the type of logic circuit of delay analysis is prestored; as such, the delay analysis cannot be automatic, as required by claim 1", the Examiner reaffirms his position in the Final rejection. Hasegawa ' 168 discloses at CL1, L58-61 that the delay model storing means store information of a circuit model including logic information, connecting information and delay information of the logic circuit; at CL2, L30-35 that dely verification can be achieved by calculating the dely time from each pin to the starting point of the logic circuit and the delay time from each pin to the ending point ogf the logic circuit based on the information of the circuit model such as logic information, connecting information and dely information. The examiner interprets this to mean that logical operation information comprises delay time information which is specific to an input terminal logical state transition and a resulting logical state transition at an output terminal; the stored delay time is specific to a state transition of the pin; and that the type of logic circuit of delay analysis is prestored.